Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An apparatus comprising:

an integrated circuit comprising:

a reconfigurable processor core including a plurality of whole processor units, each unit having a clock input to control performance of the unit; and

a controller having a plurality of clock outputs each coupled to a respective clock input of one of the whole processor units, wherein the controller is configured to independently vary a clock frequency of each whole processor unit.

Claim 2 (currently amended): The apparatus of claim 1, wherein at least one of the whole processor units comprises a digital signal processor (DSP).

Claim 3 (currently amended): The apparatus of claim [[1]] 2, wherein at least another one of the whole processor units comprises a reduced instruction set computer (RISC) processor.

Claim 4 (currently amended): The apparatus of claim 1, wherein each whole processor unit is configured to be dynamically managed on a per-task basis.

Claim 5 (currently amended): The apparatus of claim 1, wherein each whole processor unit is configured to be clocked at the lowest rate possible to reduce peak power dissipation, reduce average power dissipation, or minimize buffer memory size and power.

Claim 6 (currently amended): The apparatus of claim 1, wherein the controller is configured to generate a plurality of clock signals, each independently rate controlled to each of the whole processor ~~unit~~ units.

Claims 7-18 (cancel)

Claim 19 (currently amended): The apparatus of claim 1, further comprising a buffer coupled between an output of a first one ~~two~~ of the plurality of whole processor units and an input to a second one of the plurality of whole processor units.

Claim 20 (previously presented): The apparatus of claim 19, wherein the buffer is a first-in-first-out (FIFO) buffer.

Claim 21 (currently amended): The apparatus of claim 1, wherein the integrated circuit further comprises a first radio frequency wireless transceiver coupled to the plurality of whole processor units.

Claim 22 (currently amended): The apparatus of claim 21, wherein the integrated circuit further comprises a second radio frequency wireless transceiver coupled to the plurality of whole processor units.

Claim 23 (currently amended): The apparatus of claim 21, wherein the plurality of whole processor units and the first radio frequency wireless transceiver are on a single substrate.

Claim 24 (currently amended): A system comprising:

a display; and

an integrated circuit on a single substrate coupled to the display, the integrated circuit comprising:

a digital portion including:

a plurality of processor units, each unit having a clock input to control performance of the unit;

a controller having a plurality of clock outputs each coupled to a respective clock input of one of the plurality of processor units, wherein the controller is configured to vary a clock frequency of each processor unit; and

an analog portion including:

a first radio frequency wireless transceiver coupled to the plurality of processor units.

Claim 25 (currently amended): The system of claim 24, wherein the integrated circuit further comprises a second radio frequency wireless transceiver coupled to the plurality of processor units.

Claim 26 (currently amended): The system of claim [[23]] 24, further comprising a buffer coupled between an output of a first one ~~and a second one~~ of the plurality of processor units and an input to a second one of the plurality of processor units.

Claim 27 (currently amended): A method comprising:

generating a plurality of clock signals on an integrated circuit, each of the plurality of clock signals variable under control of a controller on the integrated circuit; and

providing each of the plurality of clock signals to a corresponding one of a plurality of processor units of a reconfigurable processor core on the integrated circuit.

Claim 28 (previously presented): The method of claim 27, further comprising varying at least one of the plurality of clock signals using the controller.

Claim 29 (cancel)

Claim 30 (previously presented): The method of claim 27, further comprising independently rate controlling each of the plurality of clock signals.

Claim 31 (currently amended): The method of claim 27, further comprising providing a clock signal controlled by the controller to a radio frequency wireless transceiver on the integrated circuit.

Claim 32 (new): The apparatus of claim 1, wherein the plurality of whole processor units comprises at least two processor units configured to operate in parallel and at least two serial processor units coupled such that an output of the first serial processor unit is coupled to an input of the second serial processor unit.

Claim 33 (new): The apparatus of claim 32, further comprising a buffer coupled between the output of the first serial processor unit and the input of the second serial processor unit.

Claim 34 (new): The apparatus of claim 32, wherein each of the plurality of whole processor units is coupled to receive an independently controllable supply voltage.

Claim 35 (new): The apparatus of claim 33, wherein each of the plurality of whole processor units and the buffer are coupled to receive an independently controllable supply voltage.